REMARKS/ARGUMENTS

Claims 1-44 are pending in this application, Claims 1, 22, 43 and 44 are amended.

Claims 1-9, 19-30 and 41-44 are rejected under 35 U.S.C. 103(a) as being obvious over Tseng et al. (U.S. Patent 6,009,256) in view of Kolchinsky et al. (U.S. Patent 5,535,406).

Applicants submit that all of the pending claims are patentable over the cited references, and reconsideration and allowance of these remaining claims are respectfully requested.

Amended independent claims 1, 43 and 44 include, among other limitations, "mapping said plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators..." Applicants respectfully submit that the cited references alone or in combination do not disclose or suggest the recited limitations.

Rather Tseng et al. is directed towards electronic design automation (EDA) systems and software for designing and verifying user's custom circuit designs. For example, as illustrated in FIGS. 4 and 6, the system of Tseng et al. "in conjunction with the user, selects the components for hardware models; that is, of the universe of possible hardware components that can be implemented in the hardware model of the user's circuit design, some hardware components will not be modeled in

hardware for a variety of reasons..." (Tseng et al., col. 18, line 66 - col. 19, line 4).

Tseng et al. then "maps the selected hardware models into a reconfigurable hardware emulation board. In particular, step 307 takes "the netlist and maps the circuit design into specific FPGA chips." (Tseng et al., col. 19, lines 14-20). Tseng et al further teaches that "step 309 generates the configuration files for mapping the hardware model to FPGA chips. In essence, step 309 assigns circuit design components to specific cells or gate level components in each chip." (Tseng et al., col. 19, lines 55-61).

Thus, Tseng et al. converts an electronic circuit design into a software model and simulates/emulates the performance of that circuit to improve the circuit design. Tseng does not however, disclose or suggest mapping a plurality of kernel sections into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators as recited in claims 1, 43 and 44 of the present invention.

Kolchinsky describes a virtual processor with a reconfigurable, programmable logic array for processing data in accord with a hardware encoded algorithm. Likewise, Kolchinsky does not teach or suggest the above limitation required by the independent claims 1, 43 and 44.

Applicants therefore respectfully submit that independent claims 1, 43 and 44 are novel and unobvious over the cited references and are therefore allowable. Applicants further

submit that claims 2-21 that depend directly or indirectly from claim 1 are allowable as is claim 1 and for additional limitations recited therein.

Similarly, amended independent claim 22 includes, among other limitations, "a plurality of hardware dependent executable code derived from said kernel sections for execution on said plurality of hardware accelerators; and a matrix describing said hardware accelerators and said executable code configured to support run time execution." Applicants submit that Tseng, and Kolchinsky, alone or in combination do not disclose or suggest the above-recited limitation.

Rather as argued above with respect to claims 1, 43 and 44 Tseng et al. converts an electronic circuit design into a software model and simulates/emulates the performance of a that circuit to improve the circuit design. Tseng et al. then maps the selected hardware models into a reconfigurable hardware emulation board. Tseng et al. does not, however, disclose or suggest a plurality of hardware dependent executable code derived from said kernel sections for execution on said plurality of hardware accelerators as recited in claim 22 of the present invention.

Applicants therefore submit that claim 22 recites a novel and unobvious system over the cited references and is therefore allowable. Applicants further submit that claims 23-42 that depend directly or indirectly from claim 22 are allowable as is claim 22 and for additional limitations recited therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
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